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We desire information on

- ☐ Memory elements
- ☐ Memory stacks
- ☐ Memory systems
  - ☐ Ferrite core
  - ☐ Plated wire

Our capacity requirement is

_____ wo

x _____ bits

Our use is

- ☐ Buffer
- ☐ Main frame memory
- ☐ Extended main memory
- ☐ Bulk core storage

Preliminary Data Sheet

Plated Wire NDRO Memory Element 40JS21

Fast memory cycle time
Nondestructive readout
High creep and crawl thresholds
Useful bipolar outputs
Low write thresholds

Lockheed Electronics Company

Preliminary Data Sheet
Plated Wire NDRO Memory
Element 40JS21

1. General

The plated wire memory element is a nickel-iron thin film electro-deposited onto a five mil diameter beryllium copper wire substrate. The deposition takes place on a continuous plating line where the substrate wire is electropolished, copper plated, and coated with the magnetic film. The film is subsequently annealed to improve its stability with respect to time. The wire passes through test stations which are capable of determining skew, dispersion, magnetostriction, and memory characteristics. Errors are detected and fed through a delay to a mechanical cutter. The wire is cut to predetermined length with bad elements discarded.

The element so produced gives NDRO memory operation with equal word current for read and write. High speed operation is achieved through the thin film nature of the element. Creep is prevented through the use of a doublet ('bipolar') digit write current. The element has low write current requirements and high disturb thresholds. Useful bipolar output levels are achieved in the NDRO mode.

The wire specification is written for a specific word strap geometry, cycle time, and write mode. The specification will change if the word straps are altered. It is possible to utilize this wire in different single or multi-turn word strap configurations. Operation at timing other than that specified is also possible.

2. Memory Element Test Specification (TA = 25°C)

This test simulates the worst case write, read, and disturb conditions a wire memory element undergoes in a normal NDRO memory operation. Each wire is 100% tested to the procedure described below

a. Word Strap

A two turn word strap is used. Each turn is ten mils wide and the spacing between the two turns is five mils. The center to center spacing between word strap pairs is 50 mils. Figure 1 shows the word strap arrangement.

b. Test Station Schematic

Figure 2 shows a schematic of the pulse test station.

c. Test Program

The test program is shown in Figure 3.

Fig. 1 Word strap configuration

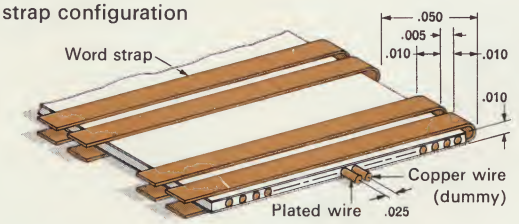

Fig. 2 Pulse test schematic

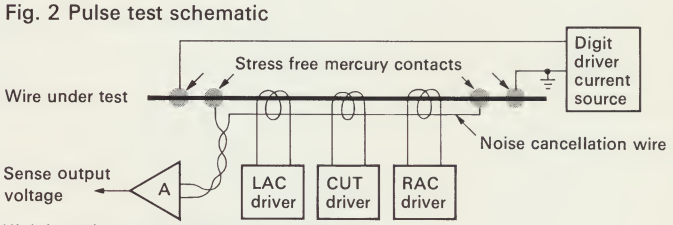

Fig. 3 Test program

Program step / Program channel	Hard history 'O'	Soft write 'I'	Undistb read uV_1	Creep disturb LAC	Creep disturb RAC	Crawl disturb CUT	Disturb read dV_1	Hard history 'I'	Soft write 'O'	Undistb read uVo	Creep disturb LAC	Creep disturb RAC	Crawl disturb CUT	Disturb read dVo
CUT word I_{w1}	⊥					⊥		⊥					⊥	
CUT word I_{w2}		⊥	⊥				⊥		⊥	⊥				⊥
LAC word I_{w1}	⊥			⊥				⊥			⊥			
RAC word I_{w1}	⊥				⊥			⊥				⊥		
Hard digit I_{d1}	⊥			⊥	⊥			⊥			⊥	⊥		
Soft digit I_{d2}		⊥							⊥					
Crawl digit I_{d3}						⊤							⊥	
No. of repeats	100	1	1	10^4	10^4	10^4	1	100	1	1	10^4	10^4	10^4	1

continued other side

Preliminary Data Sheet

Plated Wire NDRO Memory Element 40JS21

Lockheed Electronics Company

Lockheed Electro

Data Produc

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A division of Lockheed Aircraft Corporation

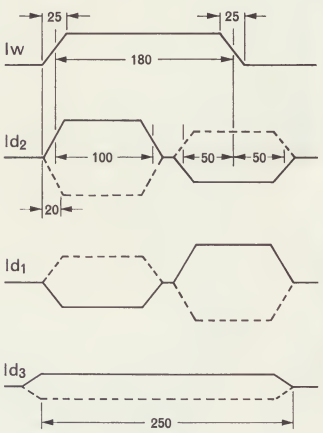
d. Current Timing
The timing relationships of the current waveforms are shown in Figure 4.
e. Current Amplitudes
I_w = Nominal word current = 450 ma
$I_{w1} = I_w + 10\% I_w$ = 495 ma
$I_{w2} = I_w - 10\% I_w$ = 405 ma
I_d = Nominal doublet digit current = 40 ma
(Digit currents are of opposite phase for writing one or writing zero and are unbalanced to the limits specified for I_{d1} and I_{d2})
$I_{d1} = I_d + 15\% I_d$ = 46 ma
$I_{d2} = I_d - 15\% I_d$ = 34 ma
I_{d3} = Digit current during crawl disturb = 2 ma
f. Peak Sense Signals
For the conditions described, the wire element must have the following output signal peak amplitudes.

$|uV| \geq 7.0$ mv

$\frac{dV}{uV} \geq 0.75$

3. Other Parameters (TA = 25°C)
All tests in Section 3 are done on an AQL basis.
a. Pulse Test
The tests performed in Figure 3 are repeated on a stationary wire with each disturb repeated more than 10^6 times.
Section 2f. must be passed.
b. Skew
Skew as defined in Section 4 should not exceed ±30 millioersteds.
c. Magnetostriction
The skew induced by a twist of 10°/inch of wire shall be no greater than 125 millioersteds.
d. Resistance
DC Resistance/Ft.
1.6 ± 0.1 ohms/ft.
e. Aging
The undisturbed and disturbed outputs of a sample are recorded. Two sections of the sample are then magnetized circumferentially to opposite polarities. The sample is then heated in a 160°C air ambient for 4 hours in a 3 oresteds axial DC field. Using the pulse tests as described in Section 2, there shall be no more than 20% degradation in either undisturbed or disturbed outputs, i.e.—

Fig. 4 Current timings



0.8 |uV| (before aging)
≤ |uV| (after aging)
0.8 |dV| (before aging)
≤ |dV| (after aging)

4. Wire Length
The wire will be supplied in lengths of 20 inches or less.

5. Definitions
uV
The peak undisturbed read output voltages from a single write preceded by adverse history.
dV
The peak disturbed read output voltages after a series of disturb patterns.
Crawl
The disturb condition produced by small bit currents in the presence of a full word field.
Creep
The disturb condition produced by full bit current in the presence of a word field generated on an adjacent word strap.
Skew
The angle between the true easy axis and the expected easy axis. It is expressed in terms of the easy axis field (millioersteds) required to compensate for the skew.
Doublet digit write
A two phase digit current where the change in phase occurs after the initial rise and before the final fall of the word current.
Magnetostriction
A change in magnetic properties induced by strain.
Aging
Any degradation of memory properties with time.